CLEAN VERSION OF THE ENTIRE SET OF CLAIMS

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1. (AMENDED) An apparatus comprising:

a processor cache unit to process a cache access request from a processor core of a processor, the processor cache unit including a processor cache controller and a processor cache; and

a chipset cache controller coupled to the processor cache unit to control a chipset cache located in a chipset internally to the processor in response to the cache access request from the processor core, the chipset being external and coupled to the processor via a bus.

2. The apparatus of claim 1 wherein the chipset cache controller comprises:

a chipset cache tag store to store tags corresponding to cache lines of the chipset cache; and

a coherency controller coupled to the chipset cache tag store to maintain cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

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3. The apparatus of claim 2 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

4. The apparatus of claim 3 wherein the coherence controller comprises:

a chipset interface circuit to send control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

5. The apparatus of claim 4 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

6. The apparatus of claim 5 wherein when the type of the cache access request is a read request and the cache valid indicator is not asserted, the operation includes one of a transfer of a data read from the memory to the cache set in the chipset cache and a transfer of a data read from the memory to the processor.

7. The apparatus of claim 6 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

8. The apparatus of claim 4 wherein when the type of the cache access request is a read request and the cache valid indicator is asserted, the operation includes a transfer of a data read from the cache set to the processor.

9. The apparatus of claim 4 wherein when the type of the cache access request is a write request, the operation includes a transfer of a data from the processor to the cache set in the chipset cache.

10. The apparatus of claim 9 wherein when the cache valid indicator is not asserted, the operation further includes a transfer of the data from the processor to the memory.

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11. The apparatus of claim 9 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

12. The apparatus of claim 5 further comprising:

a snoop circuit coupled to the chipset cache tag store to check if an address snooped on the bus matches with one of entries in the chipset cache tag store.

13. The apparatus of claim 12 wherein the set identifier specifies the cache set corresponding to the one of the entries that matches the address snooped on the bus.

14. (AMENDED) A method comprising:

processing a cache access request from a processor core of a processor by a processor cache unit, the processor cache unit including a processor cache controller and a processor cache; and

controlling a chipset cache located in a chipset internally to the processor in response to the cache access request from the processor core, the chipset being external and coupled to the processor via a bus.

15. The method of claim 14 wherein controlling the chipset cache comprises:

storing tags corresponding to cache lines of the chipset cache in a chipset cache tag store; and

maintaining cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

16. The method of claim 15 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

17. The method of claim 16 wherein maintaining cache coherency comprises:

sending control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

18. The method of claim 17 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

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19. The method of claim 18 wherein when the type of the cache access request is a read request and the cache valid indicator is not asserted, the operation includes one of a transfer of a data read from the memory to the cache set in the chipset cache and a transfer of a data read from the memory to the processor.

20. The method of claim 19 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

21. The method of claim 17 wherein when the type of the cache access request is a read request and the cache valid indicator is asserted, the operation includes a transfer of a data read from the cache set to the processor.

22. The method of claim 17 wherein when the type of the cache access request is a write request, the operation includes a transfer of a data from the processor to the cache set in the chipset cache.

23. The method of claim 22 wherein when the cache valid indicator is not asserted, the operation further includes a transfer of the data from the processor to the memory.

24. The method of claim 22 wherein when the flush indicator is asserted, the operation further includes a flushing of existing data at the cache set.

25. The method of claim 18 further comprising:

checking if an address snooped on the bus matches with one of entries in the chipset cache tag store.

26. The method of claim 25 wherein the set identifier specifies the cache set corresponding to the one of the entries that matches the address snooped on the bus.

27. (AMENDED) A system comprising:

a memory to store data;

a chipset coupled to memory having a chipset cache; and

a processor coupled to the memory and the chipset via a bus, the processor including a processor core and a cache unit, the cache unit comprising:

a processor cache unit to process a cache access request from the processor core, the processor cache unit including a processor cache controller and a processor cache, and

a chipset cache controller coupled to the processor cache unit to control the chipset cache internally to the processor in response to the cache access request from the processor core.

28. The system of claim 27 wherein the chipset cache controller comprises:

a chipset cache tag store to store tags corresponding to cache lines of the chipset cache; and

a coherency controller coupled to the chipset cache tag store to maintain cache coherency among the processor cache, the chipset cache, and a memory, according to a coherence protocol.

29. The system of claim 28 wherein the coherency protocol is a modified, exclusive, share, and invalidated (MESI) protocol.

30. The system of claim 29 wherein the coherence controller comprises:

a chipset interface circuit to send control signals to the chipset according to cache state and type of the cache access request, the control signals specifying an operation performed by the chipset.

31. The system of claim 30 wherein the control signals include at least a set identifier for a cache set in the chipset cache corresponding to the cache access request, a cache valid indicator asserted when a cache line in the cache set is valid, and a flush indicator asserted when the cache line is flushed.

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32. The system of claim 31 wherein the cache unit further comprising:

a snoop circuit coupled to the chipset cache tag store to check if an address snooped on the bus matches with one of entries in the chipset cache tag store.